L Number	Hits	Search Text	DB	Time stamp
-	61830	(Computer adj System) and @ad<19991214	USPAT;	2002/04/30 09:16
			US-PGPUB	
-	29947	((Computer adj System) and @pd<19991214)	USPAT;	2002/04/29 08:23
		and (CPU or (Central adj processing adj unit) or Processor)	US-PGPUB	
_	430683	(((Computer adj System) and @pd<19991214)	USPAT;	2002/04/29 08:24
	130003	and (CPU or (Central adj processing adj	US-PGPUB	2002/04/23 00.24
		unit) or Processor)) and (Memory adj Unit)		
		or RAM or Memory		
-	27284	(((Computer adj System) and @pd<19991214)	USPAT;	2002/04/29 09:58
.		and (CPU or (Central adj processing adj	US-PGPUB	
		unit) or Processor)) and ((Memory adj Unit) or RAM or Memory)		
_	1660	(((((Computer adj System) and	USPAT;	2002/04/29 11:44
		@pd<19991214) and (CPU or (Central adj	US-PGPUB	
		processing adj unit) or Processor)) and		
		((Memory adj Unit) or RAM or Memory)) and		
		((Circuit adj Board) or PCB or (Memory adj		
_	7	Module))) and (Signal adj5 line\$1) (((((Computer adj System) and	HCDATT.	2002/04/20 00:45
	·	(((((Computer ad) System) and   (pd<19991214) and (CPU or (Central ad)	USPAT; US-PGPUB	2002/04/29 08:45
		processing adj unit) or Processor)) and	130 13102	
		((Memory adj Unit) or RAM or Memory)) and	1	
		((Circuit adj Board) or PCB or (Memory adj		
		Module))) and (Signal adj5 line\$1) ) and		
	1943	(none near10 ground) ((Computer adj System) and @ad<19991214)	HCDAM.	2002/04/29 08:46
_	1943	and (Memory adj Module)	USPAT; US-PGPUB	2002/04/29 08:46
_	532		USPAT;	2002/04/29 10:09
		and (Memory adj Module) and (PCB or	US-PGPUB	
		(Circuit adj Board))		
-	1	(((Computer adj System) and @ad<19991214)	USPAT;	2002/04/29 08:51
		and (Memory adj Module) and (PCB or	US-PGPUB	
		(Circuit adj Board))) and (parallel\$1 adj Signal\$1 adj Line\$1)		
_	3712		USPAT;	2002/04/29 08:59
		and (CPU or (Central adj processing adj	US-PGPUB	
		unit) or Processor)) and ((Memory adj		
		Unit) or RAM or Memory)) and ((Circuit adj	1	ļ
_	307	Board) or PCB or (Memory adj Module)) (Computer adj System) and @ad<19991214 and	HCDAT.	2002/04/29 09:01
_	307	Rambus	USPAT; US-PGPUB	2002/04/29 09:01
_	118	((Computer adj System) and @ad<19991214	USPAT;	2002/04/29 09:02
		and Rambus) and (Signal\$1 adj Line\$1)	US-PGPUB	
-	11	(((Computer adj System) and @ad<19991214	USPAT;	2002/04/29 09:04
İ		and Rambus) and (Signal\$1 adj Line\$1)) and	US-PGPUB	
_	500	(ground\$1 same process\$3)	HCDATT.	2002/04/29 09:05
-	500	(((Computer adj System) and @ad<19991214 and Rambus) and (Signal\$1 adj Line\$1)) and	USPAT; US-PGPUB	2002/04/29 09:05
		(ground\$1 same process\$3) or (nonground or	1 2 2 2 2 2 2 2	
		non-ground)		A =10
-	11		USPAT;	2002/04/29 09:05
		and Rambus) and (Signal\$1 adj Line\$1)) and	US-PGPUB	
		((ground\$1 same process\$3) or (nonground		
_	27297	or non-ground)) (((Computer adj System) and @pd<19991214)	USPAT;	2002/04/29 10:30
i	21271	and (CPU or (Central adj processing adj	US-PGPUB	
		unit) or Processor)) and ((Memory adj		
ļ		Unit) or RAM or DRAM or Memory)		
- !	168		USPAT;	2002/04/29 10:13
	a F	(signal adj line\$1)	US-PGPUB	2002/04/29 10:14
-	25	(PCB and (multilayer or multi-layer) and (signal adj line\$1)) and (parallel adj2	USPAT; US-PGPUB	2002/04/29 10:14
		line\$1)	00 10100	
	104	((((Computer adj System) and @pd<19991214)	USPAT;	2002/04/29 10:31
į.		and (CPU or (Central adj processing adj	US-PGPUB	
		unit) or Processor)) and ((Memory adj		
j		Unit) or RAM or DRAM or Memory)) and		
		Rambus	<u> </u>	

Page 1

-	13	(PCB and (multilayer or multi-layer) and (signal adj line\$1)) and Rambus	USPAT; US-PGPUB	2002/05/01 07:59
-	1	(PCB and (multilayer or multi-layer) and (signal adj line\$1)) and Rambus and	USPAT; US-PGPUB	2002/04/29 13:02
-	18	(Signal\$1 adj Rout\$4) PCB same ((first adj signal) same (second	USPAT;	2002/04/29 13:34
1 -	2	<pre>adj signal)) PCB same ((first adj signal) same (second adj signal)) and Rambus</pre>	US-PGPUB USPAT; US-PGPUB	2002/04/29 11:35
-	4	Rambus and ((memory adj unit) same (memory adj controller))	USPAT; US-PGPUB	2002/04/29 11:38
-	173	(((((Computer adj System) and @pd<19991214) and (CPU or (Central adj	USPAT; US-PGPUB	2002/04/29 11:45
	1	processing adj unit) or Processor)) and ((Memory adj Unit) or RAM or Memory)) and ((Circuit adj Board) or PCB or (Memory adj Module))) and (Signal adj5 line\$1) and (PCB and Rout\$3)	USPAT;	2002/04/29 11:53
-	1	<pre>(((((((Computer adj System) and @pd&lt;19991214) and (CPU or (Central adj processing adj unit) or Processor)) and ((Memory adj Unit) or RAM or Memory)) and ((Circuit adj Board) or PCB or (Memory adj Module))) and (Signal adj5 line\$1) and (PCB and Rout\$3)) and ((first adj signal) same (second adj signal))</pre>	US-PGPUB	2002/04/29 11.33
_	91	PCB and ((MCU or Memory adj Control adj Unit) same (Memory or (Memory adj Unit) or RAM or Dram))	USPAT; US-PGPUB	2002/04/29 11:56
-	5	(PCB and ((MCU or Memory adj Control adj Unit) same (Memory or (Memory adj Unit) or RAM or Dram)) ) and ((first adj signal)	USPAT; US-PGPUB	2002/04/29 12:12
_	184	same (second adj signal)) PCB same signal same rout\$5	USPAT; US-PGPUB	2002/04/29 12:13
-	2	(PCB same signal same rout\$5) same multi-layer and ((first adj signal) same (second adj signal))	USPAT; US-PGPUB	2002/04/29 13:31
-	17	multi-layer same (data adj bus)	USPAT; US-PGPUB	2002/04/29 12:26
-	2	single-layer same (data adj bus)	USPAT; US-PGPUB	2002/04/29 12:26
_	971	rambus	USPAT; US-PGPUB	2002/04/29 12:45
_	735	rambus and bus	USPAT; US-PGPUB	2002/04/29 12:46
-	2	memory adj repeater adj hub	USPAT; US-PGPUB	2002/04/29 13:02
_	1	PCB and ((first adj signal) same (second adj signal)) same ("same" adj layer)	USPAT; US-PGPUB USPAT;	2002/05/01 08:08
_	109	connection same (MCU same Memory) (connection same (MCU same Memory)) and	US-PGPUB USPAT;	2002/04/29 13:29
1	219	PCB (computer adj system) and motherboard and	US-PGPUB USPAT;	2002/04/29 15:30
-	39	pcb ((computer adj system) and motherboard and	US-PGPUB USPAT;	2002/04/29 13:35
_	4130	pcb) and (MCU same Memory) (PCB or (Circuit adj Board)) and	US-PGPUB USPAT;	2002/04/29 14:23
-	12	((miltiple adj layer) or Multi-layer) ((PCB or (Circuit adj Board)) and ((miltiple adj layer) or Multi-layer)) and ((MCU or(Memory adj Controller) or (Memory adj Control adj Unit)) same ((Memory adj	US-PGPUB USPAT; US-PGPUB	2002/04/29 14:31
-	11	Unit) or RAM or DRAM))	USPAT; US-PGPUB	2002/04/29 14:40

[-		971	Rambus	USPAT; US-PGPUB	2002/04/29 14:43
-		58	Rambus and ((first adj signal) same (second adj Signal))	USPAT; US-PGPUB	2002/04/29 15:10
_		8	(Rambus and ((first adj signal) same	USPAT;	2002/04/29 15:09
			(second adj Signal))) and (PCB or (Signal adj Rout\$5))	US-PGPUB	2002/04/25 13.05
-		204	(PCB and (Signal adj Rout\$5))	USPAT; US-PGPUB	2002/04/29 15:09
_		13	((PCB and (Signal adj Rout\$5))) and	USPAT;	2002/04/29 15:10
			((first adj signal) same (second adj Signal))	US-PGPUB	
-		6	(computer adj system) and motherboard and pcb and Rambus	USPAT; US-PGPUB	2002/04/29 15:44
-		1	RAMBus and (PCB same design same bus)	USPAT; US-PGPUB	2002/04/29 16:29
-		51	RAMBus and PCB	USPAT; US-PGPUB	2002/04/29 16:44
-		7	(RAMBus and PCB) and ((First adj signal) same (Second adj signal))	USPAT; US-PGPUB	2002/04/29 16:44
-		537	(174/250).CCLS.	USPAT; US-PGPUB	2002/04/30 09:43
-		60364	439/\$.ccls.	USPAT; US-PGPUB	2002/04/30 09:32
-		22	439/\$.ccls. and Rambus	USPAT; US-PGPUB	2002/04/30 09:35
-		14	(Print\$2 adj Circuit adj Board))	USPAT; US-PGPUB	2002/04/30 09:36
-		7	174/\$.ccls. and (channel adj bus)	USPAT; US-PGPUB	2002/04/30 09:46
-		5	Bus and (trace adj topology)	USPAT; US-PGPUB	2002/04/30 09:50
-		34	361/\$.ccls. and Rambus	USPAT; US-PGPUB	2002/04/30 11:20
-		1297	neck adj down	USPAT; US-PGPUB	2002/04/30 11:21
-		73	parallel same (neck adj down)	USPAT; US-PGPUB	2002/04/30 11:22
-		38	439/\$.ccls. and ((neck adj down) or neckdown or neck-down)	USPAT; US-PGPUB	2002/04/30 11:42
-		1	(439/\$.ccls. and ((neck adj down) or neckdown or neck-down)) and PCB	USPAT; US-PGPUB	2002/04/30 11:53
-		1	5/5 adj rout\$4 adj rule\$1	USPAT; US-PGPUB	2002/04/30 13:23
-		7	PCB and ((neck adj down) or neck-down or neckdown)	USPAT; US-PGPUB	2002/04/30 13:29
-		36	PCB and ((Signal adj line\$1) and (equal adj width))	USPAT; US-PGPUB	2002/04/30 14:26
-	116	270	PCB and ("5" adj mil\$1)	USPAT; US-PGPUB	2002/04/30 14:27
-		161	(PCB and ("5" adj mil\$1)) and width\$1	USPAT; US-PGPUB	2002/04/30 14:28
-		110	((PCB and ("5" adj mil\$1)) and width\$1) and pattern	USPAT; US-PGPUB	2002/04/30 14:28
-		49	((PCB and ("5" adj mil\$1)) and width\$1) AND ROUT\$5	USPAT; US-PGPUB	2002/04/30 14:29
-		49	((PCB and ("5" adj mil\$1)) and width\$1) AND ROUT\$5	USPAT; US-PGPUB	2002/04/30 14:29
-		13	(PCB and (multilayer or multi-layer) and (signal adj line\$1)) and Rambus	USPAT; US-PGPUB	2002/05/01 07:59
-		13	(PCB and (multilayer or multi-layer) and (signal adj line\$1)) and Rambus	USPAT; US-PGPUB;	2002/05/01 08:00
1				EPO; JPO; DERWENT;	
			non and ((Single add almost)) come (accord)	IBM_TDB	2002/05/01 00:10
-	•	1	PCB and ((first adj signal) same (second adj signal)) same ("same" adj layer)	USPAT; US-PGPUB;	2002/05/01 08:10
			and any angles	EPO; JPO;	
-				DERWENT; IBM TDB	
1		1			

-	33	331	((circuit near3 board) or board or layer)	USPAT;	2002/05/01 11:11
	1	- 1	same (memory or Rambus) same (memory near3	US-PGPUB;	
		- 1	<pre>control\$3) same (line or connect\$4)</pre>	EPO; JPO;	
				DERWENT;	
	]		(24)	IBM_TDB	2002/05/01 11:35
-	1	4/	(Memory adj unit) same ((memory adj	USPAT; US-PGPUB;	2002/05/01 11:35
			controller) or ((memory adj control adj	JPO;	
!			unit) or MCU)) same (Signal adj line\$1)	DERWENT	
1_		2	((Memory adj unit) same ((memory adj	USPAT;	2002/05/01 11:01
i -		-	controller) or ((memory adj control adj	US-PGPUB;	2002,00,01 11.01
ĺ		1	unit) or MCU)) same (Signal adj line\$1))	JPO;	
1		ŀ	and (first adj (pin or connect\$3 or pad or	DERWENT	
			terminal))		
-		1	(((circuit near3 board) or board or layer)	USPAT;	2002/05/01 11:12
	ļ		same (memory or Rambus) same (memory near3	US-PGPUB;	
		I	<pre>control\$3) same (line or connect\$4) ) and</pre>	EPO; JPO;	
į		1	(((Memory adj unit) same ((memory adj	DERWENT;	
1		1	controller) or ((memory adj control adj	IBM_TDB	
1		1	unit) or MCU)) same (Signal adj line\$1))		
			and (first adj (pin or connect\$3 or pad or		
			terminal)))	110000	0000/05/01 11 03
-		3	(((circuit near3 board) or board or layer)	USPAT; US-PGPUB;	2002/05/01 11:23
			<pre>same (memory or Rambus) same (memory near3 control\$3) same (line or connect\$4) ) and</pre>	EPO; JPO;	
			((Memory adj unit) same ((memory adj	DERWENT;	
			controller) or ((memory adj control adj	IBM TDB	
			unit) or MCU)) same (Signal adj line\$1))	***-**	
l _		12	RAMbus adj memory adj control\$5	USPAT;	2002/05/01 11:48
Ì				US-PGPUB;	
1			·	JPO;	
ì				DERWENT	
-	524	445	memory adj control\$3	USPAT;	2002/05/01 11:51
		- 1		US-PGPUB;	
		i		JPO;	
			1 100 1 100	DERWENT	2002/05/01 12:07
-		2	(memory adj control\$3) and (memory adj	USPAT; US-PGPUB;	2002/05/01 12:07
		İ	repeater adj hub)	JPO;	
				DERWENT	
_	7.0	942	((Personal adj computer) or PC ) and	USPAT;	2002/05/01 12:08
	'-	772	(memory adj control\$3)	US-PGPUB;	
		ĺ	(Memozi aaj contezez,c,	JPO;	
		į		DERWENT	
-	17	725	(((Personal adj computer) or PC ) and	USPAT;	2002/05/01 12:10
			(memory adj control\$3)) and (PCB or	US-PGPUB;	
			(printed adj circuit adj board) or	JPO;	
	49		(circuit adj board) or motherboard)	DERWENT	0000/05/04 10 15
-	11	149	((((Personal adj computer) or PC ) and	USPAT;	2002/05/01 12:12
		İ	(memory adj control\$3)) and (PCB or	US-PGPUB;	
			(printed adj circuit adj board) or	JPO; DERWENT	
1			(circuit adj board) or motherboard)) and	DEKWENT	
1		1	((memory adj controller) or MCU or (memory adj control adj unit))		
		90	(((((Personal adj computer) or PC ) and	USPAT;	2002/05/01 12:14
-		50	(memory adj control\$3)) and (PCB or	US-PGPUB;	== == , = = , = =
			(printed adj circuit adj board) or	JPO;	
			(circuit adj board) or motherboard)) and	DERWENT	
			((memory adj controller) or MCU or (memory		
		ĺ	adj control adj unit))) and (multi-layer		
			or (multi adj layer\$2) or (multiple adj		
1			layer\$2))		

					0000 /05 /01	10.00
-		74	((((((Personal adj computer) or PC ) and	USPAT;	2002/05/01	12:39
	1	1	(memory adj control\$3)) and (PCB or	US-PGPUB;		
			(printed adj circuit adj board) or	JPO; DERWENT		
	ŀ		(circuit adj board) or motherboard)) and ((memory adj controller) or MCU or (memory	DEKWENI		
1		}	adj control adj unit))) and (multi-layer			
l	1	1	or (multi adj layer\$2) or (multiple adj			
	i	ļ	layer\$2))) and (MCU or (memory adj			
1			controller) or memory adj control adj			
	i		unit) same ((memory adj device) or (memory			
	ŀ		adj unit) or DRAM or RAM or RIMM)			
_		5	(((((Personal adj computer) or PC ) and	USPAT;	2002/05/01	12:45
			(memory adj control\$3)) and (PCB or	US-PGPUB;		
		1	(printed adj circuit adj board) or	JPO;		
	ļ		(circuit adj board) or motherboard)) and	DERWENT		
			((memory adj controller) or MCU or (memory			
	- 1		adj control adj unit))) and (multi-layer			
		i	or (multi adj layer\$2) or (multiple adj			
	-	014	layer\$2))) and Rambus PC same motherboard	USPAT;	2002/05/01	12.47
-	- 1	814	PC same motherboard	US-PGPUB;	2002/05/01	14.11
1		ļ		JPO;		
		1		DERWENT		
_		78	(PC same motherboard) and PCB	USPAT;	2002/05/01	12:47
[				US-PGPUB;		
		Į.		JPO;		
		X I		DERWENT		
-		38	((PC same motherboard) and PCB) and	USPAT;	2002/05/01	12:52
Ì			(multi\$20)	US-PGPUB;		
				JPO;		
	ł	_ ]		DERWENT	2002/05/01	12.56
-	}	3	(personal adj computer) same (motherboard	USPAT; US-PGPUB;	2002/05/01	12:50
	-		adj design)	JPO;	1	
	1			DERWENT	:	
_	l	300	motherboard same PCB	USPAT;	2002/05/01	12:58
-	i	300	motherboard bame 102	US-PGPUB;		
				JPO;		
				DERWENT		
-	1	145	(motherboard same PCB) and multip\$5	USPAT;	2002/05/01	12:58
				US-PGPUB;		
				JPO; DERWENT		
	1	_ '	DCD come (multiple adi		2002/05/01	13.00
_	1	1	motherboard same PCB same (multiple adj	USPAT; US-PGPUB;	2002/03/01	13.00
	1		layer\$3)	JPO;	1	
				DERWENT		
_	ļ	1	multiple adj layer adj motherboard	USPAT;	2002/05/01	13:10
	ļ	-		US-PGPUB;	1	
	į			JPO;		
				DERWENT	0000 105 15	
1 -	İ	1135	(174/260).CCLS.	USPAT;	2002/05/01	13:13
	1			US-PGPUB;	1	
1				EPO; JPO; DERWENT		
		4.4	174/260.ccls. and motherboard	USPAT;	2002/05/01	13.12
_	1	41	1/4/200.CCIS. and motherboard	US-PGPUB;	2002,03,01	10.16
	1			EPO; JPO;		
				DERWENT	1	
_	ĺ	19	174/260.ccls. and (multiple adj layer)	USPAT;	2002/05/01	15:31
İ	İ			US-PGPUB;	1	
1	į			EPO; JPO;		
				DERWENT		
-		5	("4910643"   "5249098"   "5278524"	USPAT	2002/05/01	13:16
-			"5396397"   "5557502").PN.	, , and	2002/05/05	15.20
į -	;	18	174/\$.ccls. and Rambus	USPAT;	2002/05/01	13:30
Ī	İ			US-PGPUB; EPO; JPO;		
1	1			DERWENT		
1	i			DEVAPRI	1	

-	1267	Rambus	USPAT;	2002/05/01 15:36
1			US-PGPUB;	
			EPO; JPO;	
1			DERWENT	
-	353	Rambus same control\$3	USPAT;	2002/05/01 15:39
}			US-PGPUB;	
			EPO; JPO;	
			DERWENT	
-	83	(Rambus same control\$3) and @pd<20000101	USPAT;	2002/05/01 15:53
			US-PGPUB;	
	]		EPO; JPO;	
		l	DERWENT	
-	83	(Rambus same control\$3) and @pd<19991230	USPAT;	2002/05/01 15:53
			US-PGPUB;	
			EPO; JPO;	
	1	5.6	DERWENT	0000/05/00 00 11
-	1	5/5 adj routing adj rule\$2	USPAT;	2002/05/02 08:11
			US-PGPUB	<u> </u>

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